TABLE 1. System Configuration Parameter Set Content(Continued)

Req	Item	Description
1-13	Output Node Output Gates	These items control the level of the Output Node Output Gates. These are specified for each CCD.
1-14	Output Node Bias Offsets	These items control the bias level applied to the Output Nodes. These are specified for each CCD.
1-15	Scuppers	These items control the bias-level to the Scuppers. These are specified for each CCD.
1-16	Back-Junction Diodes	These items select the levels of the Back Junction Diodes. These are specified for each CCD.
1-17	Bakeout Mode Switch	This item controls whether or not bakeout mode is enabled.
1-18	Focal Plane Temperature Set Point (Coarse and Fine)	These items set the focal plane temperature.

TABLE 1. System Configuration Parameter Set Content

Req	Item	Description
1-1	DEA CCD-Controller Power Selection	This items selects which CCD Controller boards within the DEA are powered on.
1-2	FEP Power Selection	This item selects which Front End Processors are powered on.
	The remaining parameters consist of DEA board settings. In order to reduce the volatility of the software to changes in the DEA hardware design, the DEA parameter settings are implemented by the software as an array of DEA register settings, leaving the final register function designations up to the DEA hardware specification.	
1-3	Image Section Phase Clocks High Levels	These items control the high level of the Image Section Phase Clocks. The ACIS software loads these levels into the Driver board's clock conditioning Digital-to-Analog converters. These are specified for each CCD.
1-4	Image Section Phase Clocks Low Levels	These items control the low level of the Image Section Phase Clocks. The ACIS software loads these levels into the Driver board's clock conditioning Digital-to-Analog converters. These are specified for each CCD.
1-5	Framestore Phase Clocks High Levels	These items control the high level of the Framestore Phase Clocks. The ACIS software loads these levels into the Driver board's clock conditioning Digital-to-Analog converters. These are specified for each CCD.
1-6	Framestore Phase Clocks Low Levels	These items control the low level of the Framestore Phase Clocks. The ACIS software loads these levels into the Driver board's clock conditioning Digital-to-Analog converters. These are specified for each CCD.
1-7	Serial Output Register Phase Clocks High Levels	These items control the high level of the Serial Output Shift Register Phase Clocks. The ACIS software loads these levels into the Driver board's clock conditioning Digital-to-Analog converters. These are specified for each CCD.
1-8	Serial Output Register Phase Clocks Low Levels	These items control the low level of the Serial Output Shift Register Phase Clocks. The ACIS software loads these levels into the Driver board's clock conditioning Digital-to-Analog converters. These are specified for each CCD.
1-9	Output Node Reset Gate High Levels	These items control the high level of the Output Node Reset Gate. The ACIS software loads these levels into the Driver board's clock conditioning Digital-to-Analog converters. These are specified for each CCD.
1-10	Output Node Reset Gate Low Levels	These items control the low level of the Output Node Reset Gate. The ACIS software loads these levels into the Driver board's clock conditioning Digital-to-Analog converters. These are specified for each CCD.
1-11	Output Node Reset Diodes	These items control the level applied to the Output Node's Reset Diode. These are specified for each CCD.
1-12	Output Node Drains	These items control the levels of each of the Output Node Drains. These are specified for each CCD and Output Node.