TABLE 1. Continuous Clocking Parameter Block(Continued)

Req	Item	Description
1-14	Split Threshold Set Points	These values are only used when the Front End Selection Algorithm is in "Event Finding Mode." These values specify the threshold above which a neighboring pixel's pulse height must be to be considered as part of an event. These values are used when grading events and computing the overall energy of an event. Each of these items applies to a specific CCD output node. These values can range from 0 to 4095, and each set is indexed by FEP Id.
1-15	Ignore Bad Column Map Flag	This value is only used when the Front End Selection Algorithm is in "Event Finding Mode." This value controls whether or not to discard events on the basis of the CCDs list of bad columns.
1-16	Grading Selection Bit Map	These parameters are only used when the Front End Selection Algorithm is in "Event Finding Mode." This set of values selects which event grades to accept. Accepted events whose grade is indicated in this list shall be telemetered.
1-17	Event Amplitude Lower Bound and Range	These parameters are only used when the Front End Selection Algorithm is in "Event Finding Mode". These parameters select the minimum and maximum amplitudes of accepted events. Events whose total amplitude (see Section 3.2.3.3.12) is less than the lower bound value, or greater than or equal to the lower bound plus range are not telemetered. These field's ranges are governed by the minimum and maximum corrected event amplitudes.
1-18	Re-compute Bias Flag	This item indicates if the software must re-compute the pixel bias values prior to starting data processing.
1-19	Bias Algorithm Mode	This parameter selects either a mean or fractile bias algorithm
1-20	Bias Rejection Criteria	If the mean bias algorithm is selected, this parameter specifies the sigma rejection criteria, used to prevent pixels containing X-ray or charged particle artifacts from affecting the estimate of the bias. If the fractile algorithm is selected, this parameter specifies the index of the sorted pixel array to use to determine the bias levels. This field can range from 0 to 4095.
1-21	Compression Flag	This indicates whether or not to compress raw pixel data values prior to being telemetered.
1-22	Compression Selection	If raw pixel data compression is enabled, this item specifies which compression table to use.
1-23	Initial Frames to Ignore	This field plus 1 specifies the number of whole exposure frames that the FEP is to ignore at the start of a bias calibration that uses this parameter block. If this value is zero, each FEP will start processing all data pixels and overclocks received after the second vsync code. Science data processing, however, always ignores the first two whole exposures.
1-24	Trickle Bias Flag	This item indicates if the software must telemeter the current bias map to telemetry after it has been computed.

TABLE 1. Continuous Clocking Parameter Block(Continued)

Req	Item	Description
1-8	Reference to an explicit DEA Load	This is an optional item which allows a maintainer to by-pass the on-board SRAM/PRAM load builder, and load these areas directly. This reference points directly into BEP memory. If 0, then no explicit DEA load is to be used. If not 0, then the item points to the memory block which contains the load image to use. Post-launch DEA load images are uplinked into memory by the maintainer using the Write Memory function of the instrument (see Section 3.2.8.3.2 on page 108), or via a patch. This parameter is intended to be used by the maintainer of the instrument, and should be 0 during normal operations. The format of the referenced SRAM/PRAM load will be specified in the ACIS Instrument Software Detailed Design Specification (AS-BUILT), MIT 36-53200, and shall support different load contents for distinct DEA boards.
1-9	Front End Selection Algorithm	This item specifies whether or not the Front End Processor should supply all pixels to the Back End (Raw Mode), or only those whose center is above the current threshold and whose pulse height is greater than or equal to the (possibly summed) pixel to its left, and greater than the (possibly summed) pixel to its right (Event-finding Mode).
1-10	Threshold Set Points	These items control the minimum pulse-height above bias a pixel sum should have to be considered an event candidate. Each of these items applies to a specific CCD output node. These values can range from -4096 to 4095. These values are only used when the Front End Selection Algorithm is in Event-finding Mode. One set of four values is specified for each FEP.
1-11	Reference to Front End Processor Code	This value allows a maintainer to override the standard code and data loaded into the Front End Processor, and provide a special load for the Science Run. This reference points directly into BEP memory. If 0, then no explicit FEP load is to be used. If not 0, then the item points to the memory block which contains the load image to use. Post-launch FEP load images are uplinked into memory by the maintainer using the Write Memory function of the instrument (see Section 3.2.8.3.2 on page 108), or via a patch. This parameter is intended to be used by the maintainer of the instrument, and should be 0 during normal operations. The format of the referenced FEP Load image will be specified in the ACIS Instrument Software Detailed Design Specification (AS-BUILT), MIT 36-53200.
1-12	Event List Packing Code	This parameter is only used when the Front End Selection Algorithm is in “Event Finding Mode”. This value is not used when the Front End is processing raw pixels. This value selects the format to use when sending processed events. Currently, the following event-list formats are supported: Faint 1x3 and Graded 1x3.
1-13	Reference to a 1-D Window Collection	An observer uses this item to specify a set of 1-dimensional event selection and processing windows to use for the Science Run. If no windows are specified, Continuous Clocking Mode shall process all events from the CCDs using processing parameters specified in this block.

TABLE 1. Continuous Clocking Parameter Block

Req	Item	Description
1-1	Parameter Block Identifier	This item is a ground-supplied identifier which is echoed by the instrument software in key portions of the science telemetry.
1-2	FEP CCD Selection	These items specify which CCD a given FEP should process. The items are indexed by FEP Id. Any given CCD may be specified more than once in the set, at the cost of reducing the total number of CCDs being used. CCDs or FEPs which are not powered on (see Section 3.2.7 on page 99) are ignored and will not be used for the run. If there are no powered CCD being processed by a powered FEP, the science run will be aborted.
1-3	Number of Rows to Sum	This specifies the number of rows to sum prior to clocking out the output registers, expressed in powers of 2. For example, 0 means don't perform any row summation, 1 means sum 2 rows, 2 means sum 4 rows, etc. This value can range from 0 to 9 (i.e. sum a maximum of 512 rows) (NOTE: Power constraints may further restrict the total number of rows that can be summed. Such restrictions, however, do not have to be built into the instrument software).
1-4	Number of Columns to Sum	This specifies the number of pixels to sum at the Output Node prior to each transfer to the DPA, expressed in powers of 2. For example, 0 means don't perform any column summation, 1 means sum 2 columns, 2 means sum 4 columns, etc. This value can range from 0 to 6 (i.e. sum a maximum of 64 columns to ensure that each quadrant contain at least 4 columns).
1-5	Output Register Clocking Mode	This item controls the clocking mode of all of the CCD's Serial Output Shift Registers. This item can specify either Full-Mode, AC-Mode, BD-Mode or Diagnostic-Mode. See Section 2.2.2 on page 20 for a description of these modes.
1-6	Number of Overclock Pairs	This item specifies the number of extra summed pixel pairs to clock out of the Serial Output Shift Registers. Continuous Clocking Mode uses these pixel sums to determine the bias introduced in the CCD's pixel pulse height by the analog electronics. This value can range from 0 to 15 pairs of pixels.
1-7	Video Chain Responses	This item controls the response of the Video Subsection in the Detector Electronics Assembly. This item selects 1 or 4 electrons per Analog-to-Digital Unit (ADU). These items are indexed by FEP Id. If a single CCD is specified by more than 1 FEP entry, then the last corresponding chain response entry is used for the listed CCD.