c. The use of only two output nodes, such as in AC and BD mode, is selected via a discrete command to the DEA CCD controller to swap the output register phase clocks.

TABLE 1. Timed Exposure SRAM Operations

Operation	Number of SRAM Blocks	Description
Integrate	1	Do not perform any clocking operations.[a]
Image to Frame	4	Clock one row from the image array to the framestore, and from the framestore to the output registers.
Frame to OR for Discard	4	Clock one row from the framestore to the output registers, without clocking the image array.
Frame to OR	4	Clock one row from the framestore to the output registers, without clocking the image array.
OR to ON for discard (no summing)	1	Clock one pixel from the output registers to their output nodes and discard the result.[b]
OR to ON discard (x2 summing)	1	Clock two pixels from the output registers to their output nodes and discard the result.
OR to ON sample, standard	1	Clock one pixel from the output registers to their output nodes and sample the result (1 electron/ADU).
OR to ON sample, attenuated	1	Clock one pixel from the output registers to their output nodes and sample the result. Use signal timing to attenuate the signal (4 electrons/ADU).
OR to ON sample, x2, standard	1	Clock two pixels from the output registers to their output nodes, and sum and sample the pixels at the output nodes.
OR to ON sample, x2, attenuated	1	Clock two pixels from the output registers to their output nodes, and sum and sample the pixels at the output nodes.
Reverse OR to ON for discard (no summing)	1	Clock one pixel from the output registers to their opposite output nodes and discard the result.[c]
Reverse OR to ON discard (x2 summing)	1	Clock two pixels from the output registers to their opposite output nodes and discard the result.
Reverse OR to ON sample, standard	1	Clock one pixel from the output registers to their opposite output nodes and sample the result.
Reverse OR to ON sample, attenuated	1	Clock one pixel from the output registers to their opposite output nodes and sample the result. Use signal timing to attenuate the signal.
Reverse OR to ON sample, x2, standard	1	Clock two pixels from the output registers to their opposite output nodes, and sum and sample the pixels at the output nodes.
Reverse OR to ON sample, x2, attenuated	1	Clock two pixels from the output registers to their opposite output nodes, and sum and sample the pixels at the output nodes.

a. ‘Integrate’ may be identical to ‘OR to ON with discard’

b. ‘OR to ON with discard’ may be identical to ‘OR to ON sample’. The pixel code is used to tell the DPA to ignore the pixel.