TABLE 1. Continuous Clocking SRAM Operations

Operation	Number of SRAM Blocks	Description
Image to Frame	4	Clock one row from the image array to the framestore, and from the framestore to the output registers.
OR to ON discard (x2)	1	Clock two pixels from the output registers to their output nodes and discard the result.
OR to ON sum, x2	1	Clock and sum two pixels from the output registers into the output nodes.
OR to ON sample, standard	1	Clock one pixel from the output registers to their output nodes and sample the result (1 electron/ADU).
OR to ON sample, attenuated	1	Clock one pixel from the output registers to their output nodes and sample the result. Use signal timing to attenuate the gain (4 electrons/ADU).
OR to ON sample, x2, standard	1	Clock two pixels from the output registers to their output nodes, and sum and sample the pixels at the output nodes.
OR to ON sample, x2, attenuated	1	Clock two pixels from the output registers to their output nodes, and sum and sample the pixels at the output nodes.
Reverse OR to ON sum, x2	1	Clock and sum two pixels from the output registers away from their output nodes.[a]
Reverse OR to ON discard (x2 summing)	1	Clock two pixels from the output registers away from their output nodes and discard the result.
Reverse OR to ON sample, standard	1	Clock one pixel from the output registers away from their output nodes and sample the result.
Reverse OR to ON sample, attenuated	1	Clock one pixel from the output registers away from their output nodes and sample the result. Use signal timing to attenuate the gain (4 electrons/ADU).
Reverse OR to ON sample, x2, standard	1	Clock two pixels from the output registers away from their output nodes, and sum and sample the pixels at the output nodes.
Reverse OR to ON sample, x2, attenuated	1	Clock two pixels from the output registers away from their output nodes, and sum and sample the pixels at the output nodes.

a. The use of only two output nodes, such as in AC and BD mode, is selected via a discrete command to the DEA CCD controller to swap the output register phase clocks.