TABLE 1. Front End Processor Memory Map Overview

Virtual Address	Byte Size	Name	Use
0xbfc00000 aliased to portion of Auxiliary Image Data area	0x8000	Boot RAM	Contains Bootstrap loader software (see Section Section 40.0) and Microboot Control Word (see Section 4.2.1). This area MUST be loaded by the Back End Processor via the shared memory interface prior to releasing the FEPs reset line.
0xbf800000	N/A	External Debug Board	Used for developement and pre-flight testing
0xbf400000	0x30	Mongoose CSI Sub-block	see Section 4.2
0xa0c00000	12Mbits	Bias Map Memory	Stores one 12-bit bias value for each pixel in a CCD image. The bias values are set by software.
0xa0800000	12Mbits	Image Memory	Contains 12-bit image pixel values read by the FEPs image acquisition hardware
0xa0401000	0x40	Image Control Registers	see below
0xa0400000	0x18	FEP I/O Devices	see below
0xa0000000	1.5MB	Auxiliary Image Data (Bulk Memory)	Contains scratch data space, overclock pixel buffers, threshold bit-plane, bias parity error plane, BEP-to-FEP command mailbox, FEP-to-BEP request mailbox, FEP-to-BEP ring buffer. A portion of this RAM is also used for the Boot RAM area. If the Boot RAM area is used for another purpose when the system is running, the BEP is required to re-load the area prior to re-booting the FEP.
0x80080000	0x20000	Instruction Cache (SEU-immune)	Contains copy of code loaded from the BEP using a program loaded by the BEP into the FEP's Boot RAM.
0x80000000	0x20000	Data Cache (SEU-immune)	Contains data space for run-time stacks, and FEP program data.