TABLE 1. R3000 Core Instruction Set

Mnemonic	Instruction
	Co-processor Instructions
cfcz	Move from Co-processor Z Control Register
copz	Co-processor Z Operation
ctcz	Move to Co-processor Z Control Register
lwcz	Load Word to Co-processor Z Register
mfc0	Move from System Co-processor Register
mfcz	Move from Co-processor Z Register
mtc0	Move to System Co-processor Register
mtcz	Move to Co-processor Z Register
tlbp	System Co-processor Probe TLB for Match
tlbr	System Co-processor Read Indexed TLB Entry
tlbwi	System Co-processor Write Indexed TLB Entry
tlbwr	System Co-processor Write Random TLB Entry
rfe	System Co-processor Return from Exception
swcz	Store Word from Co-processor Z Register
	Load and Store Instructions
lb	Load byte
lbu	Load byte unsigned
lh	Load half-word
lhu	Load half-word unsigned
lui	Load Upper 16-bits immediate
lw	Load Word
lwl	Unaligned Load Word Left
lwr	Unaligned Load Word Right
mfhi	Move to High Accumulator (mult,div)
mflo	Move from Low Accumulator
mthi	Move to High Accumulator
mtlo	Move to Low Accumulator
sb	Store Byte
sh	Store Half-word
sw	Store Word
swl	Unaligned Store Word Left
swr	Unaligned Store Word Right
	Miscellaneous Instructions
break	Breakpoint
slt	Set on Less Than
slti	Set on Less Than Immediate
sltiu	Set on Less Than Immediate Unsigned
sltu	Set on Less Than Unsigned
syscall	System Call

TABLE 1. R3000 Core Instruction Set

Mnemonic	Instruction
	Arithmetic Instructions
add	Add
addi	Add Immediate (16-bit)
addiu	Add Unsigned Immediate
addu	Add Unsigned
and	AND
andi	AND Immediate
div	Divide
divu	Divide Unsigned
mult	Multiply
multu	Multiply Unsigned
nor	NOR
or	OR
ori	OR Immediate
sll	Shift Logical Left
sllv	Shift Logical Left Variable
sra	Shift Right Arithmetic
srav	Shift Right Arithmetic Variable
srl	Shift Logical Right
srlv	Shift Logical Right Variable
sub	Subtract
subu	Subtract Unsigned
xor	XOR
xori	XOR Immediate
	Branch and Jump Instructions
bczf	Branch Co-processor Z Flag False
bczt	Branch Co-processor Z Flag True
beq	Branch if Registers Equal
bgez	Branch if register >= 0
bgezal	Branch and Link if register >= 0
bgtz	Branch register > 0
blez	Branch register <= 0
bltz	Branch register < 0
bltzal	Branch and Link register < 0
bne	Branch if registers not equal
j	Jump
jal	Jump and Link
jlr	Jump and Link Register
jr	Jump Register