b. ‘OR to ON with discard’ may be identical to ‘OR to ON sample’, with the pixel code is used to tell the DPA to ignore the pixel.

TABLE 1. Timed Exposure SRAM Operations

Operation	Number of SRAM Blocks	Description
Integrate	1	Do not perform any clocking operations.[a]
Image to Frame	4 (TBD)	Clock one row from the image array to the framestore, and from the framestore to the output registers. TBD: Should we also clock the output registers?
Frame to OR for Discard	4 (TBD)	Clock one row from the framestore to the output registers, without clocking the image array. TBD: Should we also clock the output registers? If not, use Frame to OR instead.
Frame to OR	4 (TBD)	Clock one row from the framestore to the output registers, without clocking the image array.
OR to ON for discard (no summing)	1	Clock one pixel from the output registers to their output nodes and discard the result.[b]
OR to ON discard (x2 summing)	1	Clock two pixels from the output registers to their output nodes and discard the result.
OR to ON sample, low gain	1	Clock one pixel from the output registers to their output nodes and sample the result.
OR to ON sample, high gain	1	Clock one pixel from the output registers to their output nodes and sample the result. Use signal timing to increase gain.
OR to ON sample, x2, low gain	1	Clock two pixels from the output registers to their output nodes, and sum and sample the pixels at the output nodes.
OR to ON sample, x2, high gain	1	Clock two pixels from the output registers to their output nodes, and sum and sample the pixels at the output nodes.
Reverse OR to ON for discard (no summing)	1	Clock one pixel from the output registers to their opposite output nodes and discard the result.
Reverse OR to ON discard (x2 summing)	1	Clock two pixels from the output registers to their opposite output nodes and discard the result.
Reverse OR to ON sample, low gain	1	Clock one pixel from the output registers to their opposite output nodes and sample the result.
Reverse OR to ON sample, high gain	1	Clock one pixel from the output registers to their opposite output nodes and sample the result. Use signal timing to increase gain.
Reverse OR to ON sample, x2, low gain	1	Clock two pixels from the output registers to their opposite output nodes, and sum and sample the pixels at the output nodes.
Reverse OR to ON sample, x2, high gain	1	Clock two pixels from the output registers to their opposite output nodes, and sum and sample the pixels at the output nodes.

a. ‘Integrate’ may be identical to ‘OR to ON with discard’