TABLE 1. Continuous Clocking SRAM Operations

Operation	Number of SRAM Blocks	Description
Image to Frame	4 (TBD)	Clock one row from the image array to the framestore, and from the framestore to the output registers. TBD: Should we also clock the output registers?
OR to ON discard (x2)	1	Clock two pixels from the output registers to their output nodes and discard the result.
OR to ON sum, x2	1	Clock and sum two pixels from the output registers into the output nodes.
OR to ON sample, low gain	1	Clock one pixel from the output registers to their output nodes and sample the result.
OR to ON sample, high gain	1	Clock one pixel from the output registers to their output nodes and sample the result. Use signal timing to increase gain.
OR to ON sample, x2, low gain	1	Clock two pixels from the output registers to their output nodes, and sum and sample the pixels at the output nodes.
OR to ON sample, x2, high gain	1	Clock two pixels from the output registers to their output nodes, and sum and sample the pixels at the output nodes.
Reverse OR to ON sum, x2	1	Clock and sum two pixels from the output registers into their opposite output nodes.
Reverse OR to ON discard (x2 summing)	1	Clock two pixels from the output registers to their opposite output nodes and discard the result.
Reverse OR to ON sample, low gain	1	Clock one pixel from the output registers to their opposite output nodes and sample the result.
Reverse OR to ON sample, high gain	1	Clock one pixel from the output registers to their opposite output nodes and sample the result. Use signal timing to increase gain.
Reverse OR to ON sample, x2, low gain	1	Clock two pixels from the output registers to their opposite output nodes, and sum and sample the pixels at the output nodes.
Reverse OR to ON sample, x2, high gain	1	Clock two pixels from the output registers to their opposite output nodes, and sum and sample the pixels at the output nodes.